

RAPID1 – 8-Bit Rapid IO Endpoint Chipset

Advanced Product Brief

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3 Dec 2002

What is RapidIO

- Packet switched - point to point interconnect intended primarily as an intra-system interface, to connect processors, coprocessors, memory, and memory mapped I/O
- Low overhead & low latency optimized as an “inside-the-box”, device level interface
- Small silicon footprint can be implemented in ASICs and FPGAs
- Software transparent an extension of the microprocessor bus; allows direct, physical memory mapping of the entire machine
- Reliable delivery of packets, with detection and recovery in hardware
- Layered architecture which permits varying complexities of switch fabrics and end-points and future additions to the specifications
- IO technologies - Standard LVDS and Serial Gigabit
- Open Standard developed and promoted by the RapidIO Trade Association – <http://www.rapidio.org> (Cisco, Motorola, etc...)
- RapidIO Architecture is conceptually similar to internet protocol (IP), with similar advantages.

Specification Hierarchy

Logical Specification

- Information necessary for the end point to process the transaction.
(i.e. Transaction type, size, physical address)



Transport Specification

- Information to transport packet from end to end in the system.
(i.e. Routing Address)

Common Transport Spec

Physical Specification

- Information necessary to move packet between two physical devices.
(i.e. Electrical interface, flow ctrl)

8/16 LP-LVDS Parallel

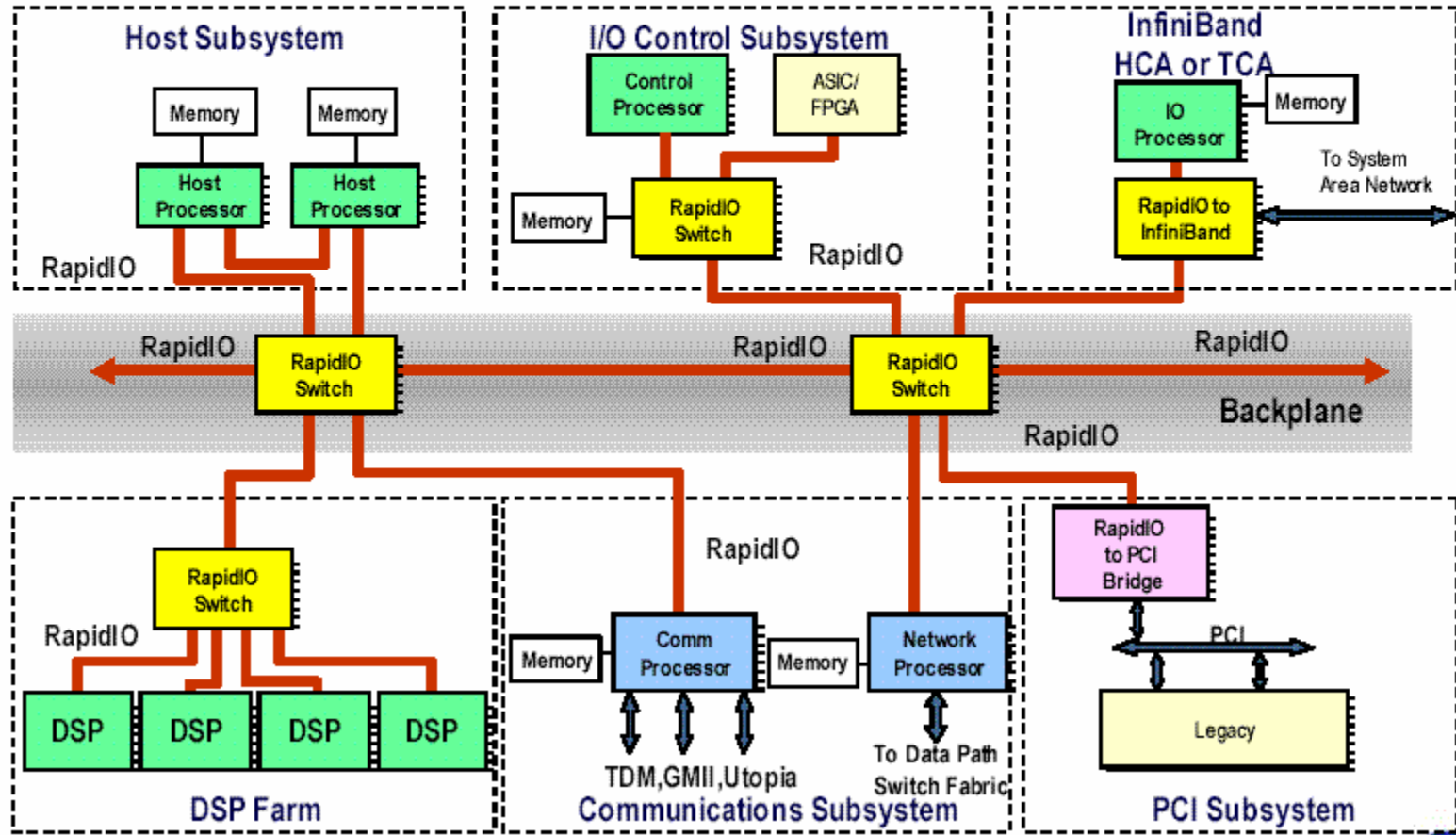
1/4 Serial

Future Physical Specs

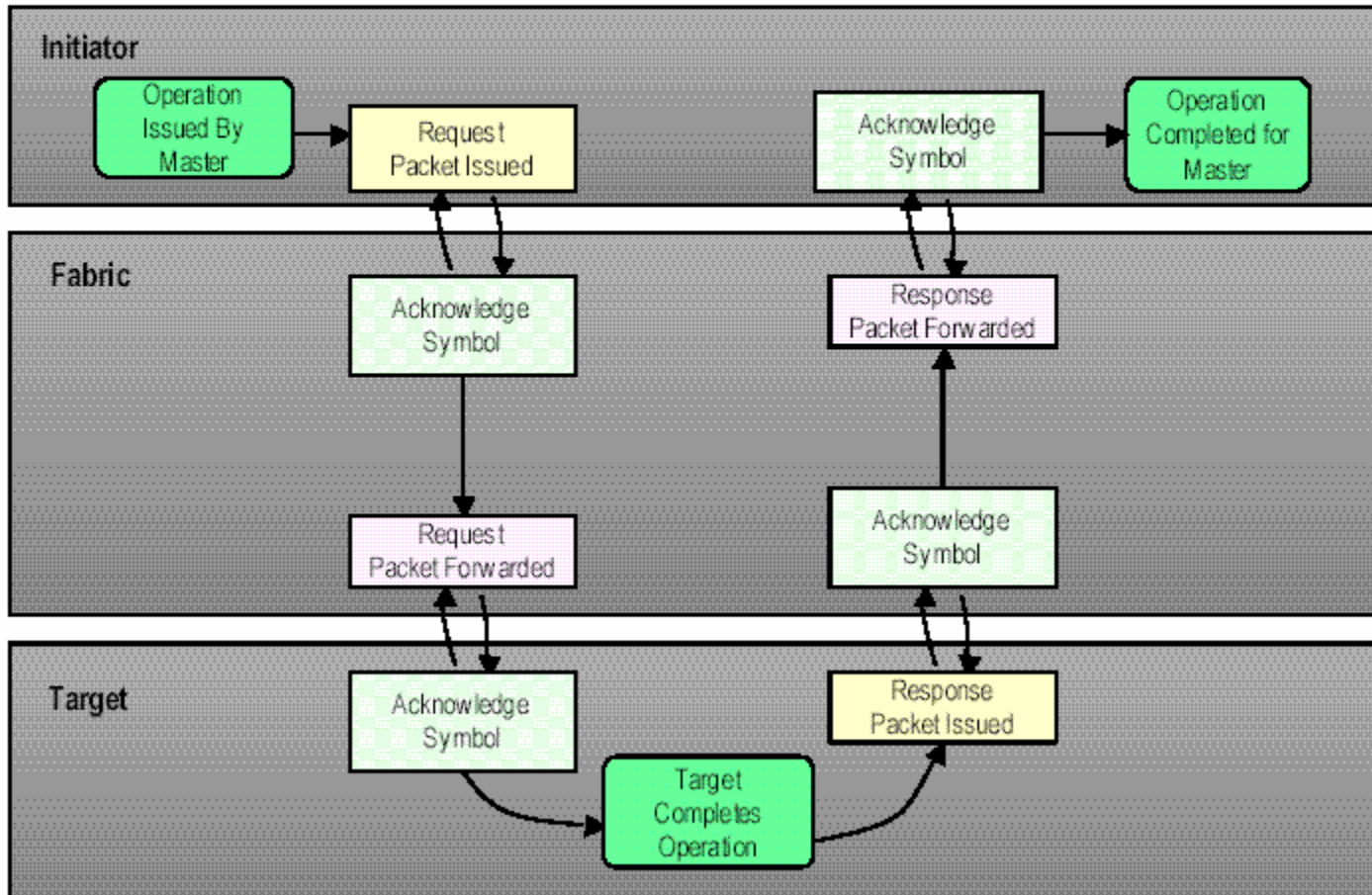
Inter-Operability Specification

Compliance Checklist

RapidIO Architecture

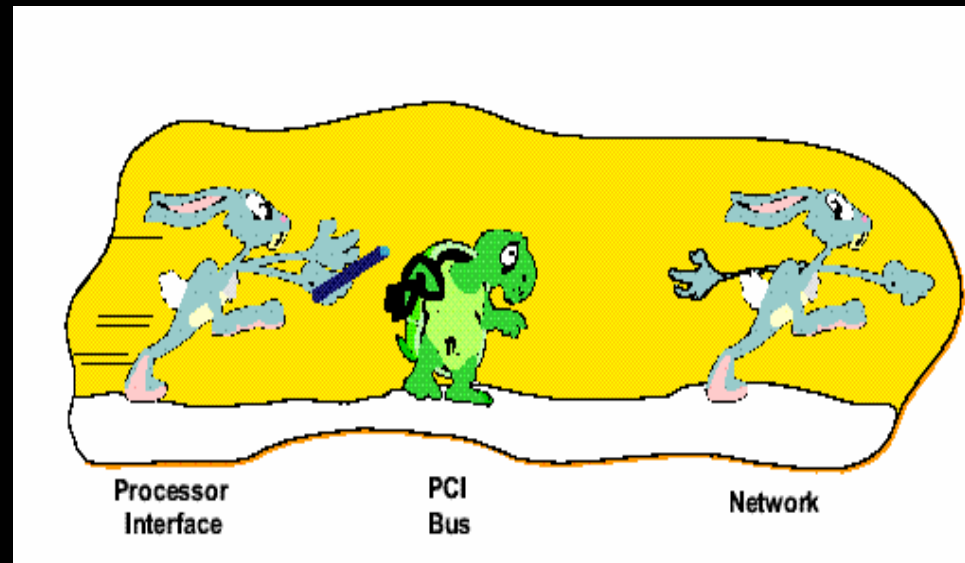


Operation Sequence

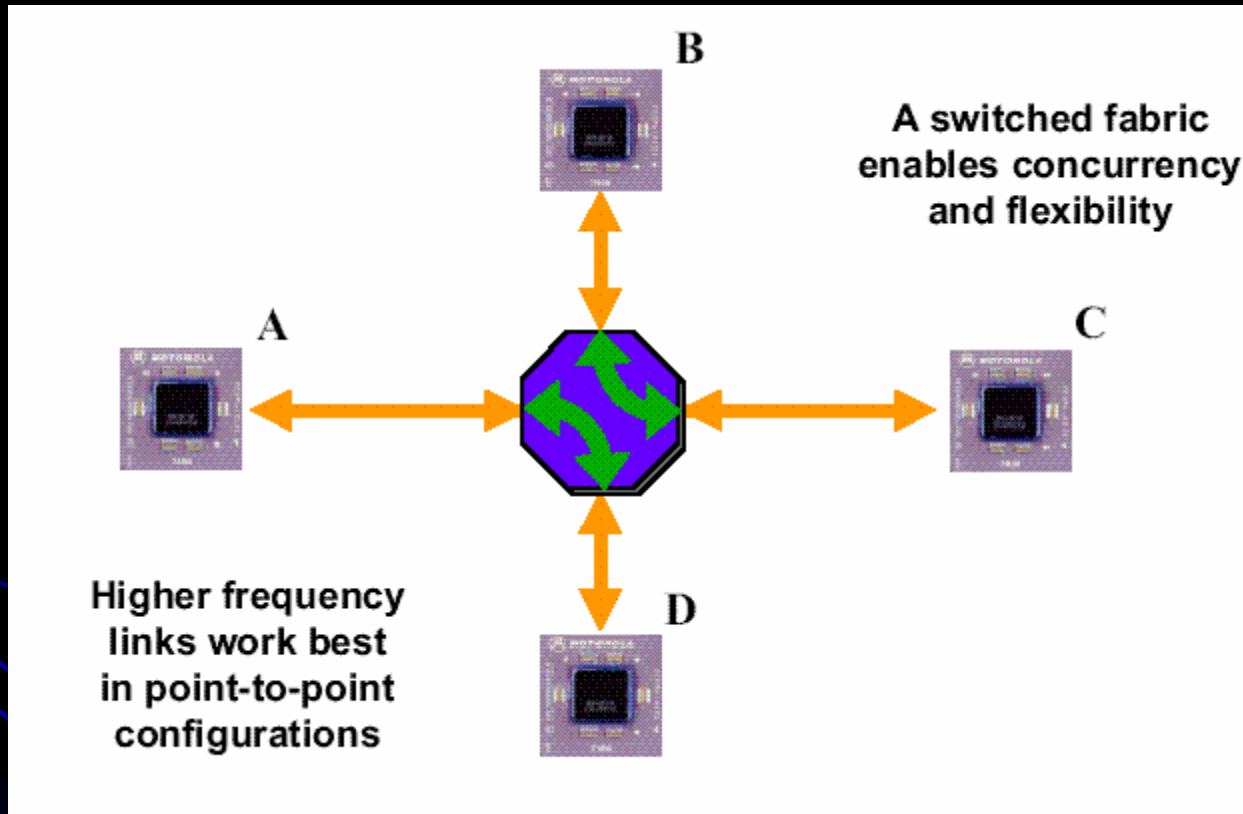


Applications of RapidIO

- This High Performance Interconnect technology is designed primarily for networking and communication markets.
- The Important bottleneck in Networking and Communication Equipment is the “speed” at which the the various components inside the box communicate with each other and the possible “concurrency” among such communications. RapidIO eliminates this bottleneck.
- RapidIO architecture offers bandwidth, software independence, fault tolerance and low latency required in the communication market.



Switching Benefits

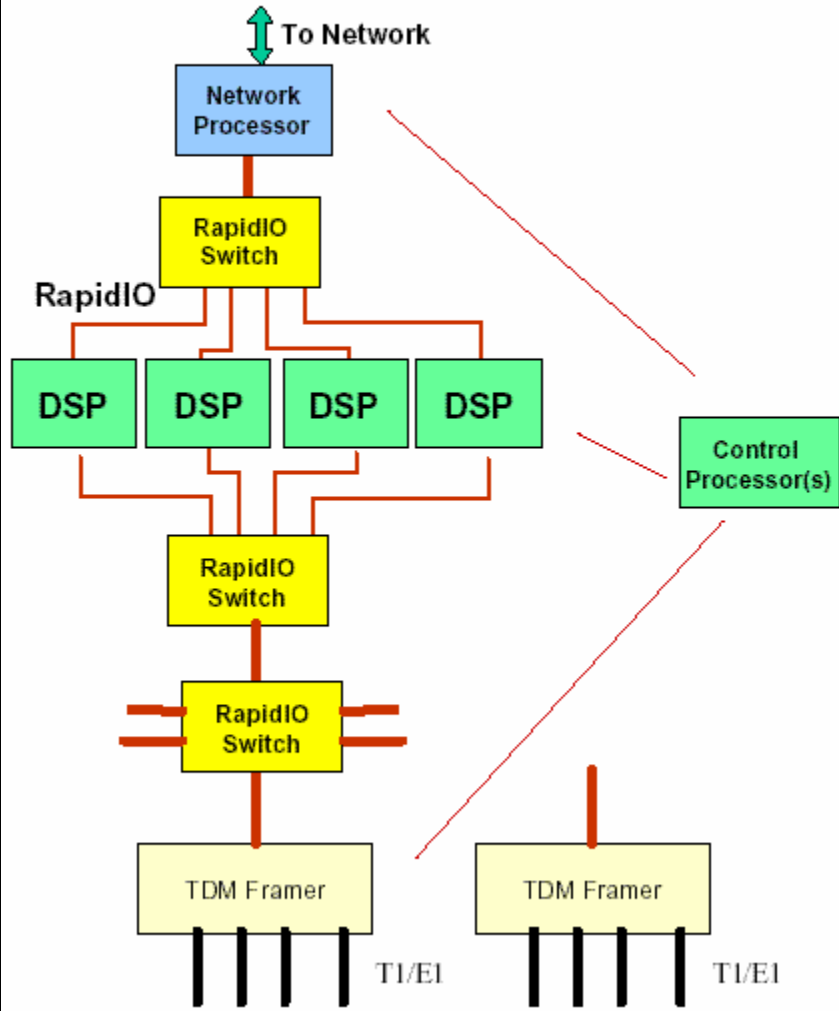


IP Telephony System

IP Packets

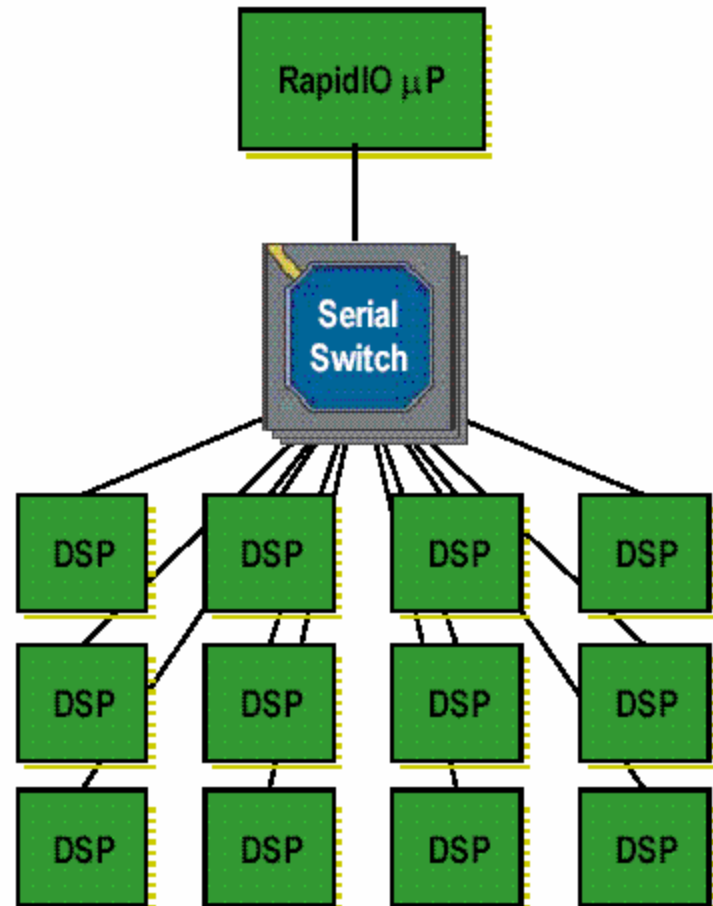
V.90, Fax, Voice

TDM



Serial RapidIO DSP Farm

- Seamless DSP Connectivity
- Effective Aggregation of Traffic
- Low Latency



Other RapidIO Products

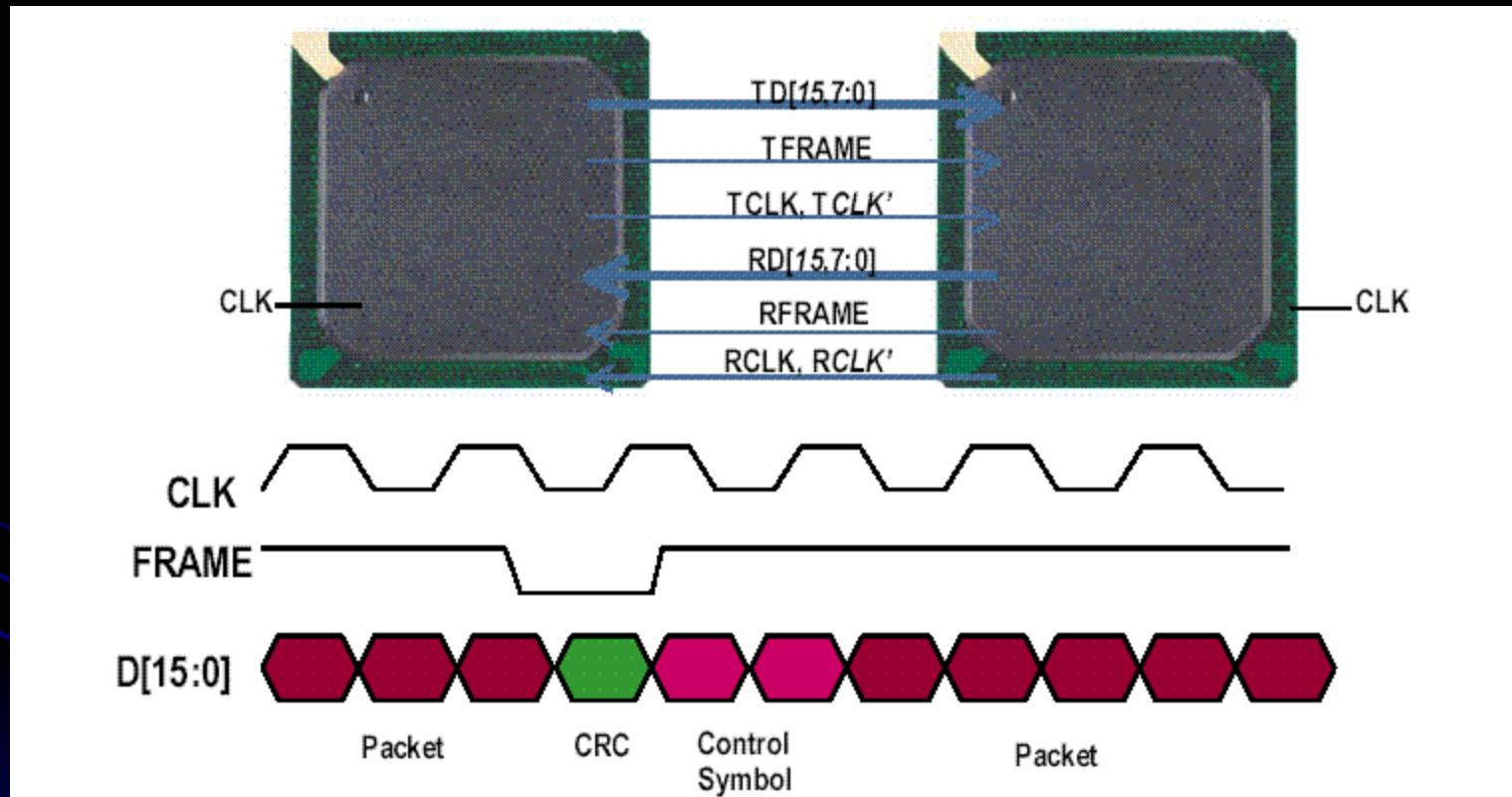
- **Motorola RapidIO Enabled Processor MPC8450, Network Processor C-10**
- **Tundra's Tsi5xx RapidIO Switching Fabrics, Tsi4xx RapidIO Bridge Devices, Tsi8xx RapidIO PowerPC Host Bridges**
- **REDSWITCH RS100116-port RapidIO Switch/Bridge**
- **Tektronix RapidIO Debug Environment**
- **8-bit Port Physical Layer Interface and Logical and Transport Layer Interface Verilog Cores from Xilinx and Altera.**

RapidIO Specifications

www.rapidio.org



RapidIO 8/16 Physical Layer Interface



RapidIO 8/16 Physical Layer Interface

- Physical Layer Interface is responsible for handling of the transmission of packets provided by logical layer, flow control, error management and other system functions between each electrically connected device pair.
- Control Symbols enable the Physical Layer Protocol to handle the flow control and error recovery at the hardware level.

S= 0	ackID	rsr=0	$\bar{S}= 1$	rsv= 00	prio
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Packet Physical Layer Field Formats

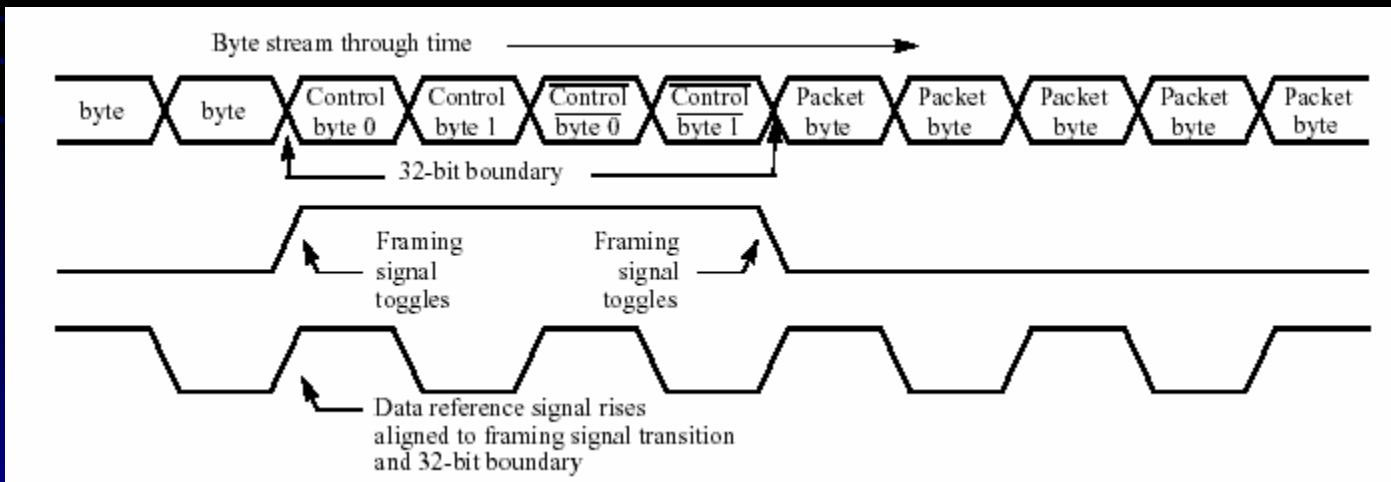
S - RapidIO request or response packet/physical layer control symbol

ackID - Packet Identifier for acknowledgments back to packet sender

prio - Sets the Packet Priority

Control Symbols

- **Physical Layer Entity**
- **16-bits (repeated inverted for robustness)**
- **Can be sent separately or inserted within the packet, delineated by the Frame.**
- **Control Symbol Types:**
 - **Acknowledgement Control Symbols(Packet-accepted, Packet-retry and packet-not-accepted)**
 - **Packet Control Symbol(IDLE, STOMP, EOP, RESTART-FROM-RETRY, THROTTLE)**
 - **Link Maintenance(Link-Request and Link Response)**



Flow Control

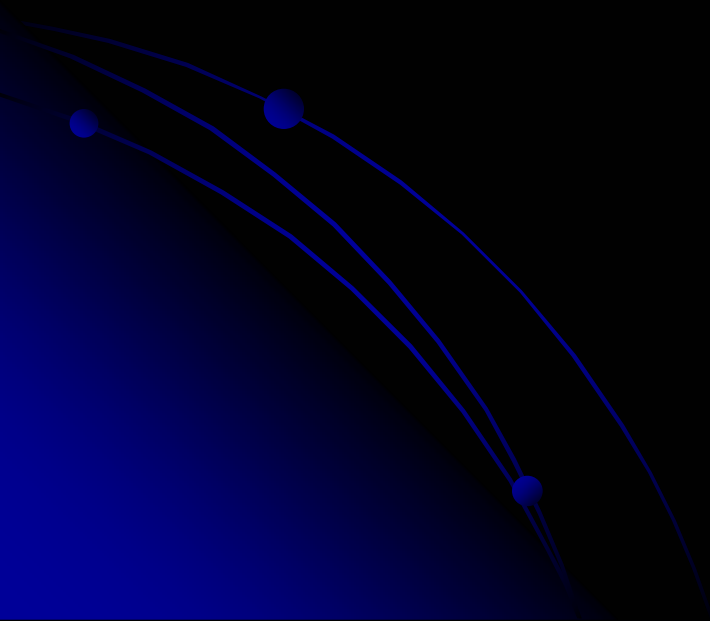
- **The flow control operates between each pair of ports connected by an LP-LVDS link. The purpose of link level flow control is to prevent the loss of packets due to a lack of buffer space in the receiver.**
- **Two Modes of Flow control**
 - **Receiver Controlled Flow Control : The Input Side of the Port controls the flow of packets on a packet by packet basis. This is Simplest and most basic method of flow control. Every RapidIO LP-LVDS port shall support receiver-controlled flow control.**
 - **Transmitter Controlled Flow Control : Here the receiving port provides information to its link partner about the amount of buffer space it has available for packet reception. With this Information, the sending port can allocate the use of receiving port's receive buffer.**

Error Management

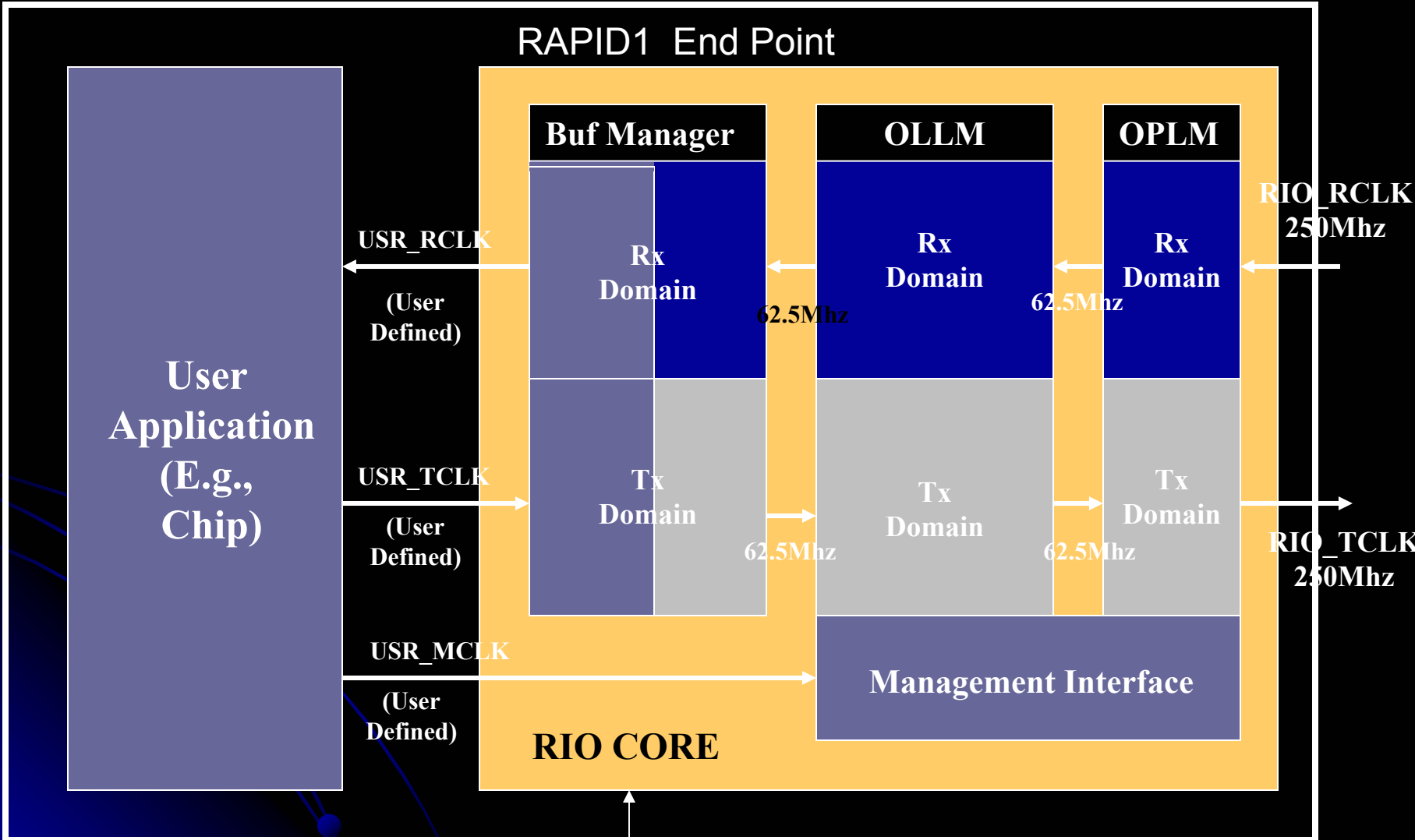
- **RapidIO 8/16 Physical Layer Protocol implements the various error detection and recovery mechanisms.**
 - **Single bit error detection**
 - **Lost Packet Detection with Timeouts**
 - **Copy of Inverted Control Symbol for error detection on the corrupt control Symbols**
 - **Fixed AckID Sequencing for detection of out of order packets and protocol violating control symbols**
 - **CRC on data packet to detect errors in data packets**

- **Recovery is Implemented through:**
 - **Hardware Retry of Corrupt packets**
 - **Physical Layer Status Request and Response Symbols**

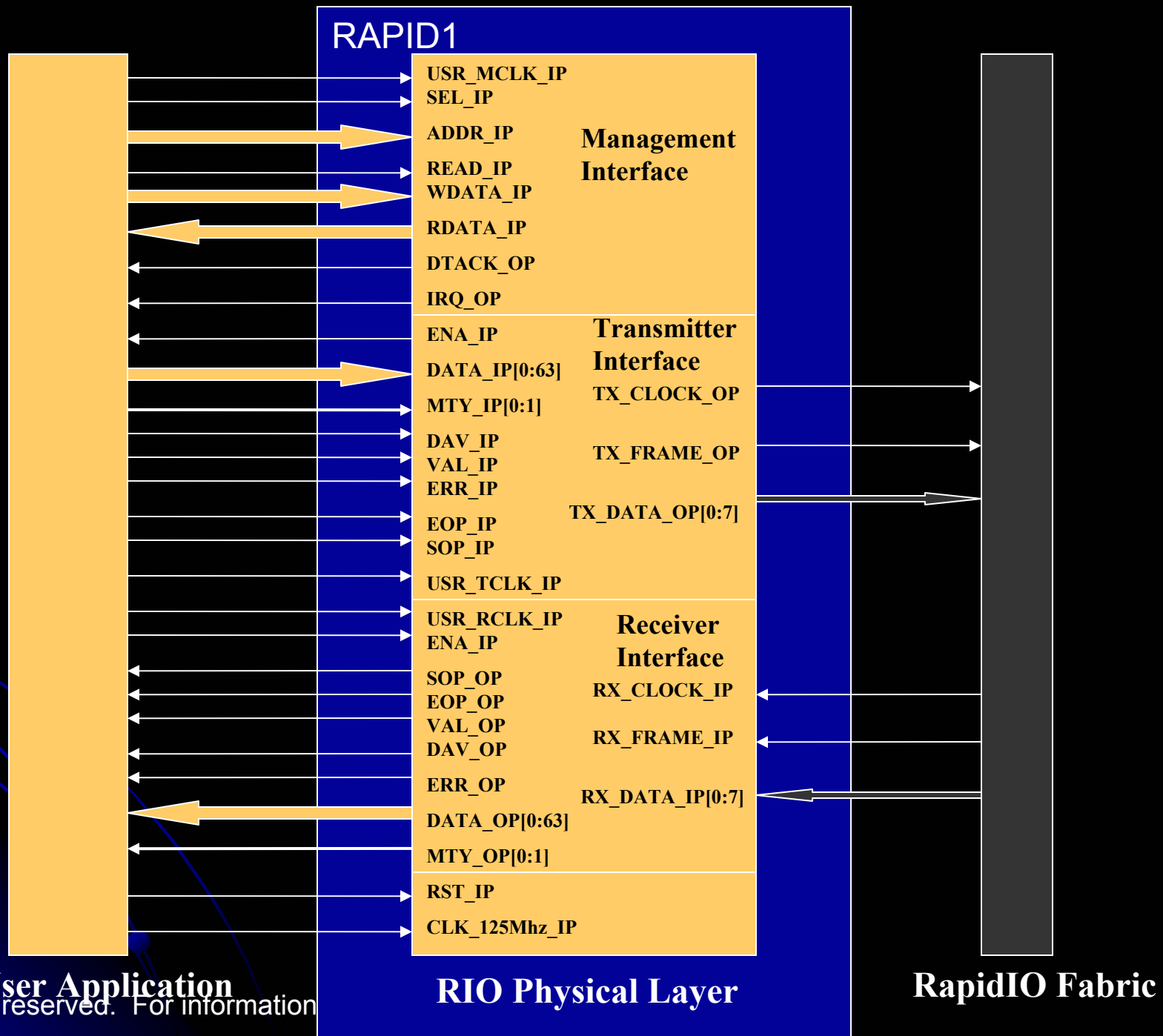
RAPID1 Architecture



Application Interface & Clock Domains

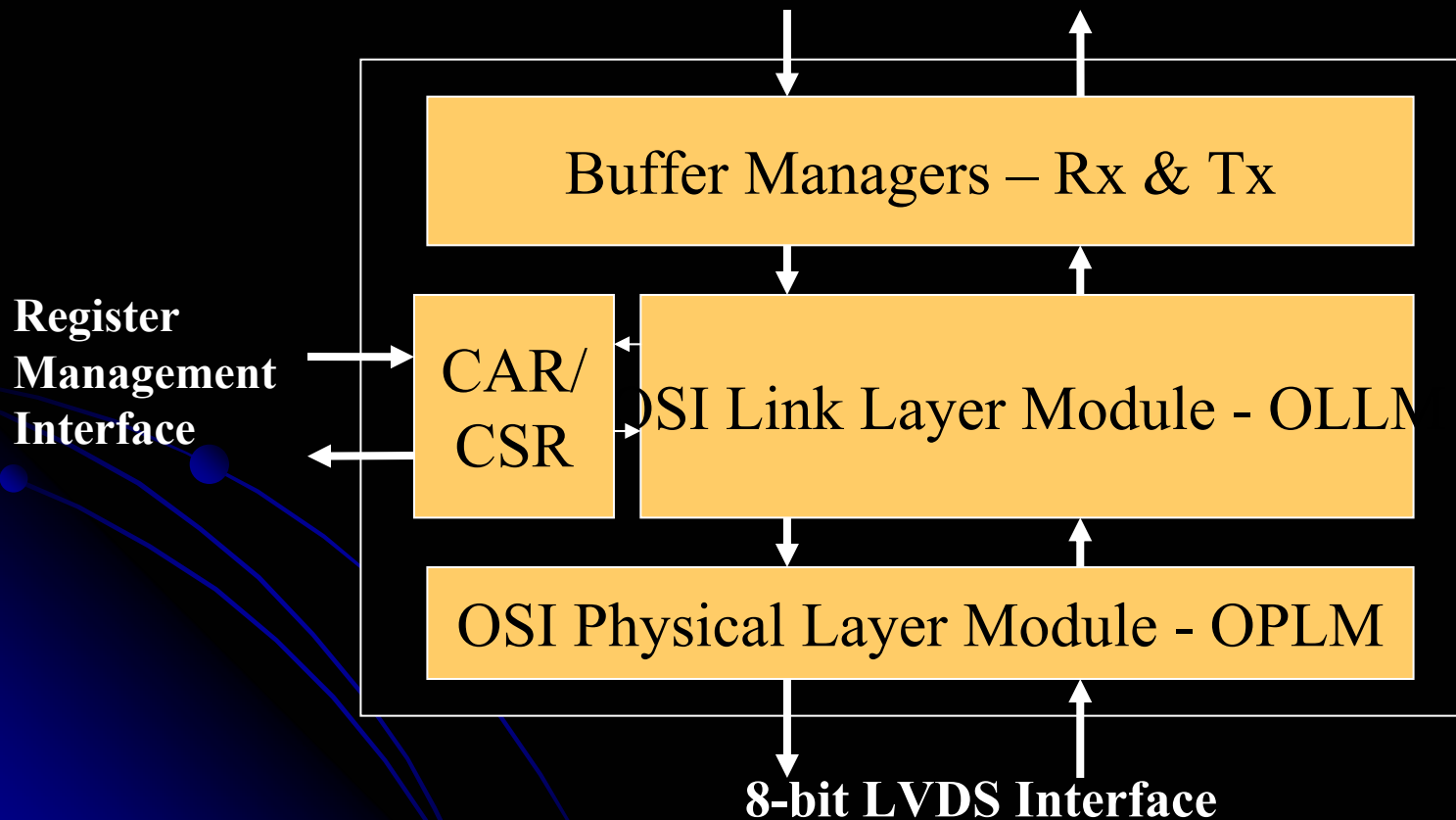


**Rapid1's
Pin-out**

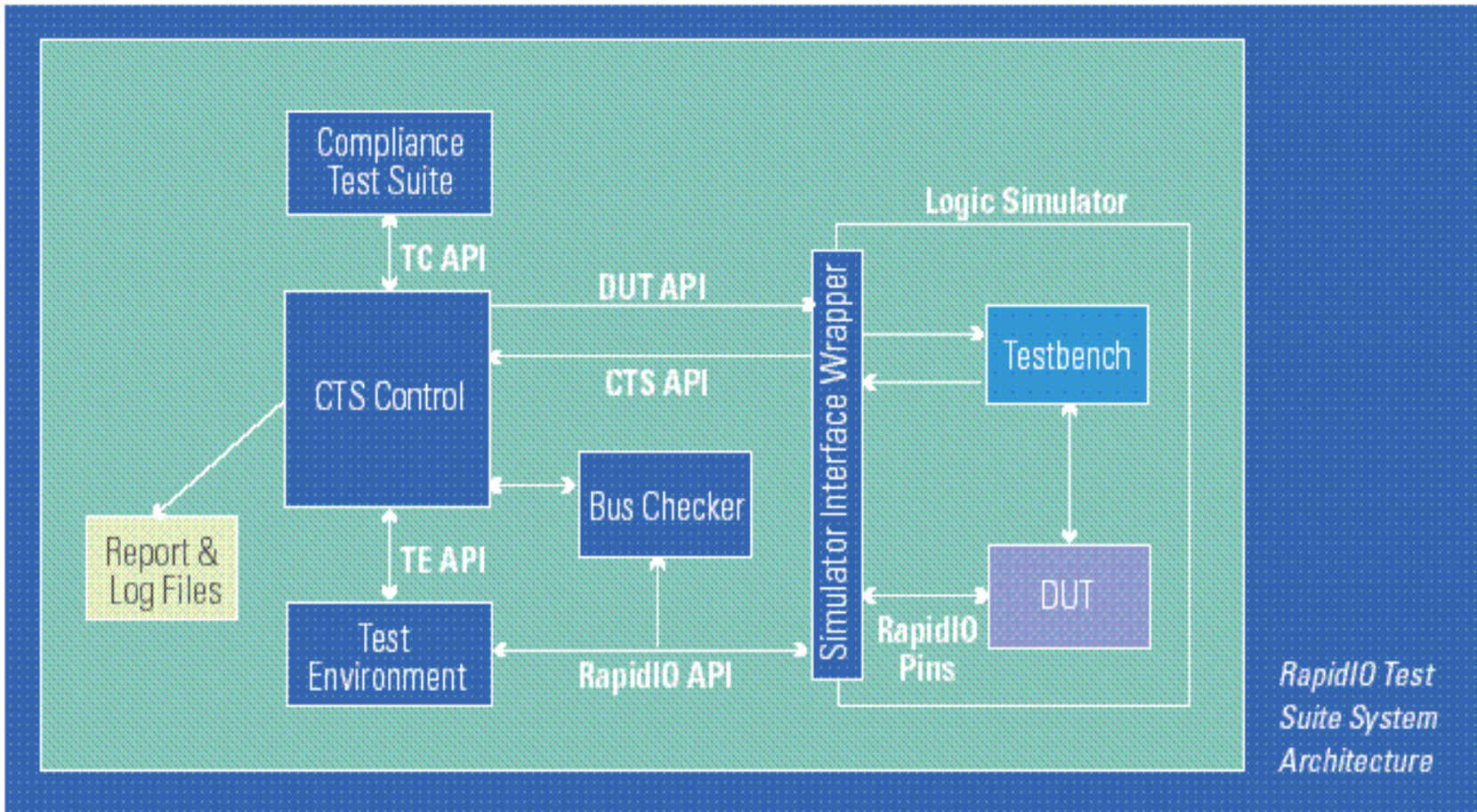


RAPID1 - RapidIO 8-bit Physical Layer Core Block Diagram

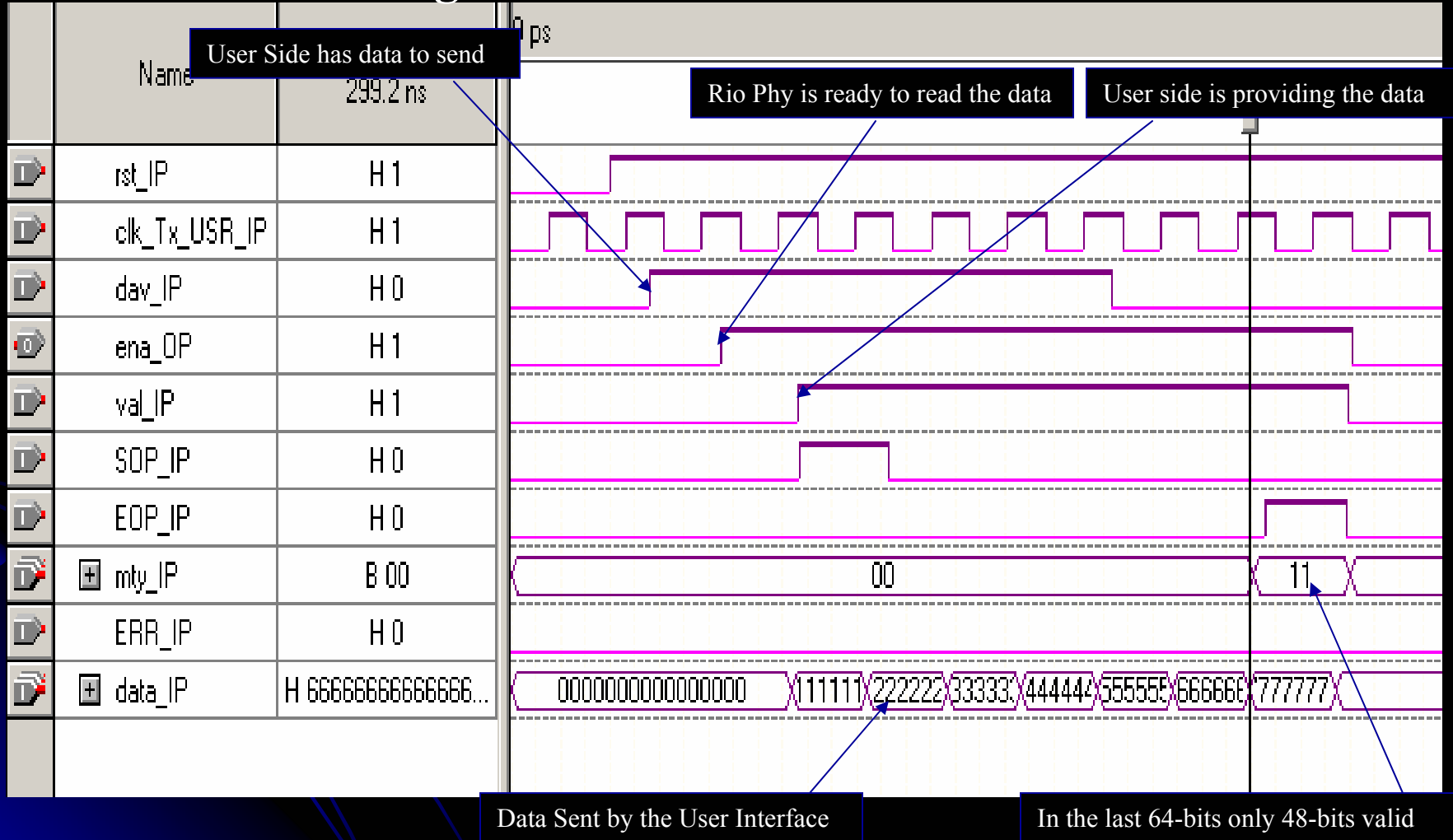
Interface for the Logical & Transport Layer



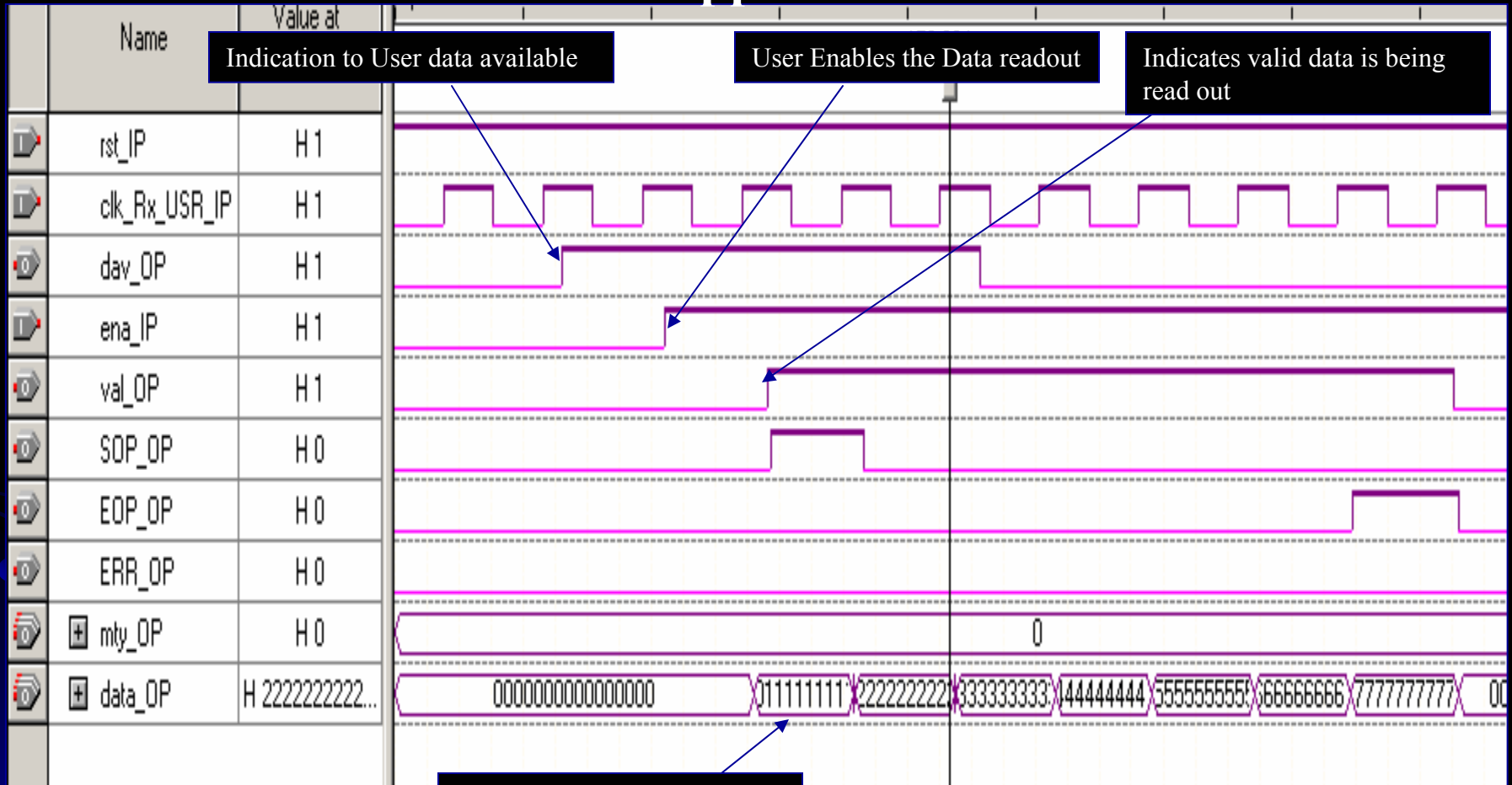
RAPID1 Testing Methodology – Uses Motorola’s RapidIO Test Bed



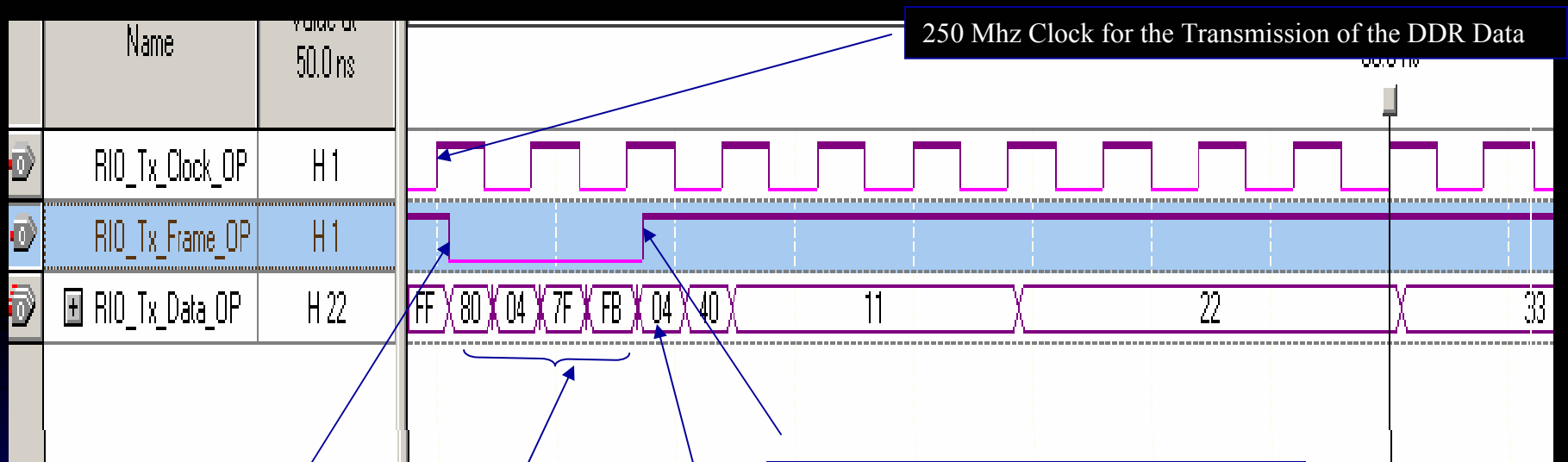
RAPID1 – Verification Results - User Application Providing Data Packet for Transmission



RAPID1 Verification - Received Packet is Provided to the User Application



DDR Data Sent out of the LVDS Interface to RapidIO Fabric



New Data Packet is being sent on to the Link

End of the Link Training

IDLE Control Symbol being sent on to the Link

DDR Data

RapidIO 8-bit Physical Layer Core Features – Compared to Competition IP

Sl.	Features	VP	XILINX	ALTERA
1.	Compliance with the RapidIO Interconnect Specification, Revision 1.2	✓	✗	✗
2.	Embedded Buffer Manager	✓	✗	✓
3.	Peak Performance 0f 8Gbps	✓	✓	✓
4.	Data Rate 250 MHz clock rate, 500Mbps per LVDS pin pair	✓	✓	✓
5.	Supports Packet Retry, stomp, transmission error recovery, throttle-based flow control and CRC	✓	✓	✓
6.	Availability of Core in VHDL	✓	✗	✗
7.	Separate Clock Domains for Receiving and Transmitting the Data	✓	✗	✓
8.	Separate Clock Domain to control Management Interface	✓	✓	✓

Summary

- RapidIO 1.2 compliant core, RAPID1, from VP Technologies, Inc. is currently undergoing detailed verification & and is expected to sample to lead customers in February/March 2003
- RAPID2 is focussing on a 1x/4x LP-serial PHY
- RAPID-F effort will target a multiport RAPIDIO fabric chipset.