

FORTHCOMING PRODUCT BRIEF

VPT1750AP Product Family



Enabling Permanent Proactive Solutions to Problems of Electronics Parts and Systems Obsolescence Through Processor & Component Emulations

Our intellectual property (IP), developed over seven years and supported in part, by USAF AFRL's EPOI initiative and US Navy's SBIR program, encompasses the problems of legacy electronic design extraction, legacy design analysis, VLSI processor and board emulations, ASIC/FPGA synthesis, SmartSupplyChain™ virtual component delivery and integration technologies, system-level virtual prototyping, validation & test, and rapid technology insertion.

Through application of our advanced design technologies, we are able to license "drop-in" chipsets that are faithful emulations of obsolete VLSI microprocessors and DSPs of complexities ranging from a few thousand gates to several million (e.g., i960, PACE1750A/AE, i860, ADSP20160, Z8001, or an obsolete PowerPC) for military use, usually in a time-frame between 12-18 months after ARO.



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FEATURES

1. All features of obsolete 1750A processors preserved

– All documented & visible features (instructions, registers/state, clock cycle and I/O) are identical to the obsolete part. Legacy binary software "drop-in" compatibility. Processors designed independently from publicly available design documentation.

2. Extensive Validation & Verification

– Extensive instruction-level tests, intensive instruction tests, non-ISA and bus-level tests, timing tests, startup/console/interrupt mode tests. Detailed validation against hardware model – cross-testing against original part.

3. Delivery and Licensing formats

– Hard and soft VHDL licenses, or as FPGA and ASICs (Contact us for details). Full system-integration & custom support for technology insertion into your legacy system.

DELIVERY SCHEDULE (MIL-STD-1750A)

- PACE1750A emulations availability (Summer 2002), PACE1750AE (Fall 2002), PACE1753/1754 (MMU/PIC) (Fall 2002).
- BX1750 emulations (Spring 2003)

Features & prices are for informational purpose only, and do not represent a promise or offer.


URL <http://www.vptinc.com>

VP TECHNOLOGIES, INC.




EMULATIONS OF OBSOLETE PROCESSORS

Focus: MIL-STD-1750A Processors

Processor Emulations (1750A Processor Family)



- Processors are compliant with MIL-STD-1750A specification
- Pin, cycle, and function accurate emulations of components from various vendors (e.g., PACE 1750A/AE, BX1750, and F9450)
- Licensed as hard or soft VHDL source formats, as FPGAs, or as ASICs



Emulations are indistinguishable from original part – preserving binary software compatibility

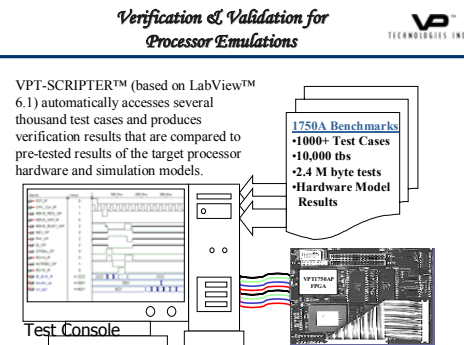
VP Technologies Inc., a Georgia ATDC Company, serves two critical defense markets; emulation of obsolete VLSI processors and the retargeting of electronic systems to newer platforms through the use of virtual prototyping. We set the bar in exceeding customer expectations, leveraging our innovative and proprietary design technologies, a professional DCAA-audited management and cost structure, combined with a 'can do' work ethic

[Our Customers]

US Air Force
Lockheed Martin Sanders
US Navy Air Command
TRW Space and Defense Electronics
Lockheed Martin Missiles and Fire Control

All trademarks are the property of their respective owners.

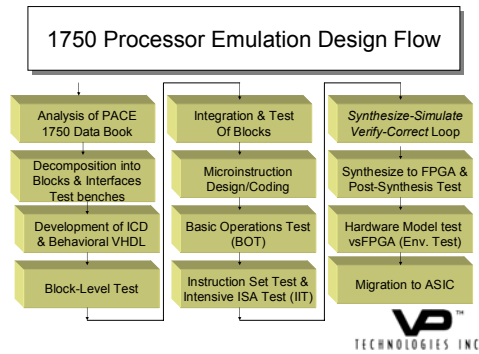
FPGA-BASED EMULATION VALIDATION METHODOLOGY



Test & Validation Approach

- FPGA emulation tested against data book and SEAFAC Test Suites.
- Tests run on the hardware modeler run against the FPGA-emulation, and any anomalies detected and included.
- Tests on the FPGA-emulation are run against the hardware modeler, and any anomalies in timing or function included.
- Application and control OFP software run on the FPAG emulation and compared with actual target system behavior. Complete behavior under all modes verified.
- Validated part is then migrated to an ASIC.
- Automated test setup using LabView 6.1™ directly interfaces with our FPGA-prototype and the internet to facility rapid turnaround on customer-generated test suites.

FPGA-BASED DEMONSTRATION AT DMSMS 2002 EXHIBITION BOOTH (MARCH 2002)



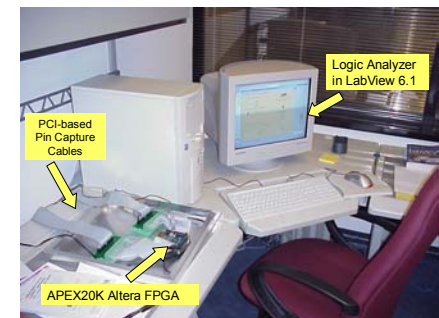
Test Demonstrations on FPGA

- **Data types, Memory Addressing & Bus-level behavior tests** – A series of tests showing formats supported and operations on them.
- **Integer Instruction Set Tests** – A series of tests showing execution of integer instructions with functionality and timing identical to that specified by the PACE 1750A and MIL-STD_1750A ISA.
- **Floating Point Instruction Set Tests** – A series of tests showing execution of the floating point instruction set with functionality and timing identical to the PACE 1750A and MIL-STD-1750A ISA.
- **Interrupt and Fault behavior tests** – Multiple tests showing maskable and non-maskable interrupts and faults as specified by PACE 1750A and MIL-STD-1750A ISA. Demonstrates extensive use of XIO and Input/Output instruction subset.
- **Console operations test** – Demonstration of console operations as per the PACE 1750A and MIL-SD-1750A ISA.

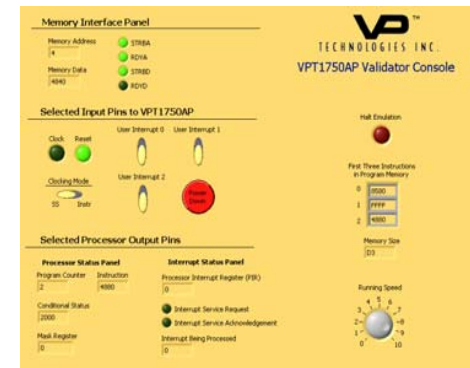
AUTOMATED EMULATION VALIDATION ENVIRONMENT

The test setup allows rapid and accurate validation of the emulation against a variety of test vectors. These test vectors are fed in via the PCI interface to the emulation mapped to an FPGA, via a virtual instrument – the logic analyzer – implemented in LabView 6.1 from National Instruments. This environment allows rapid exchange of information between a hardware modeler, such as an IMST™ tester.

Verification Setup for FPGA-based 1750A Emulation



LabView™ Based Automated Test Environment



Developing a validation and verification plan, in collaboration with our customers, helps us minimize risks on insertion of the emulation into the target system. Please contact us with your emulation requirements. Email: sales@vptinc.com